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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	6,750,605 <i>02</i>	
	Filing Date	June 15, 2004	
	First Named Inventor	Moore	
	Art Unit		
	Examiner Name		
Total Number of Pages in This Submission	6	Attorney Docket Number	MRE-7DIV

ENCLOSURES (Check all that apply)		
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT		
Firm or Individual name	Brown & Michaels PC	
Signature	<i>Megh D</i> Reg. No. 45,612	
Date	8/4/04	

CERTIFICATE OF TRANSMISSION/MAILING			
I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.			
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AUG 17 2004



Patent No. 6,750,605

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Number: 6,750,605 *b2*
Issued: June 15, 2004
Name of Patentee: Chad Byron Moore
Title of Invention: FIBER-BASED FLAT AND CURVED PANEL DISPLAYS

Commissioner of Patents and Trademarks
Washington, DC 20231
Attn: Certificate of Correction Branch

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT
FOR PTO MISTAKE (37 CFR 1.322)

1. Attached in duplicate is Form PTO/SB/44 with at least one copy being suitable for printing.
2. Attached are copies of the following:
 - First page of the present application, filed August 9, 2001
 - Page containing Col. 1 and Col. 2 of the issued patent
3. The exact page and line numbers where errors occur in the application file are:

Col. 1, lines 5-10, **REFERENCE TO RELATED APPLICATIONS**

This is a divisional patent application of application Ser. No. 09/299,371, filed Apr. 26, 1999, entitled "FRIT-SEALING PROCESS USED IN MAXING DISPLAYS", which is now U.S. Pat. No. 6,354,899 issued Mar. 12, 2002. The aforementioned patent is hereby incorporated herein by reference.

4. In the Reference to Related Applications section, the word "MAXING" should be "MAKING". A copy of the first page of the application, as filed, showing the correct wording in this section, is attached.
5. Please send the Certificate to:

Meghan Van Leeuwen
Brown & Michaels, P.C.
400 M&T Bank Building
118 North Tioga Street
Ithaca, New York 14850-4343

By: *Meghan Van Leeuwen*
Meghan Van Leeuwen, Reg. No. 45,612
Agent of Record
Date: 8/3/04

AUG 17 2004

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,750,605 B2

DATED: June 15, 2004

INVENTOR: Chad Byron Moore

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

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This is a divisional patent application of application Ser. No. 09/299,371, filed Apr. 26, 1999, entitled "FRIT-SEALING PROCESS USED IN MAKING DISPLAYS", which is now U.S. Pat. No. 6,354,899 issued Mar. 12, 2002. The aforementioned patent is hereby incorporated herein by reference.

MAILING ADDRESS OF SENDER:

Brown & Michaels
400 M&T Bank Building
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Ithaca, New York 14850-4343

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FIBER-BASED FLAT AND CURVED PANEL DISPLAYS

REFERENCE TO RELATED APPLICATIONS

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FIELD OF THE INVENTION

The invention pertains to the field of fiber-based displays and methods of manufacture. More particularly, the invention pertains to fiber-based full-color plasma, plasma addressed liquid crystal, and field emission displays and their method of manufacture.

BACKGROUND OF THE INVENTION

All electronic display technologies are composed of a large array of display picture elements, called pixels arranged in a two-dimensional matrix. Color is added to these displays by subdividing each pixel element into three-color subpixels. The electronic display technologies can be further divided into a category known as flat-panel displays. The basic structure of a flat-panel display comprises two glass plates with a conductor pattern of electrodes on the inner surfaces of each plate with additional structure to separate the plates or create a channel. The conductors are configured in a x-y matrix with horizontal and vertical electrodes deposited at right angles from each other to allow for matrix addressing. Examples of flat-panel displays include plasma displays, plasma addressed liquid crystal (PALC) displays, field emission displays (FED), and the like.

Plasma display panels (PDP) have been around for about 30 years, however they have not seen widespread commercial use. The main reasons are the short lifetime, low efficiency, and cost of the color plasma displays. Most of the performance issues were solved with the invention of the three electrode surface discharge AC plasma display (G. W. Dick, "Three-Electrode per PEL AC Plasma Display Panel", 1985 International Display Research Conf., pp. 45-50; U.S. Pat. Nos. 4,554,537, 4,728,864, 4,833,463, 5,086,297, 5,661,500, and 5,674,553). The new three electrode surface discharge structure advances many technical attributes of the display, but its complex manufacturing process and detailed structure makes manufacturing complicated and costly.

Currently, plasma display structures are built up layer by layer on specialty glass substrates using many complex processing steps. FIG. 1 illustrates the basic structure of a surface discharge AC plasma display made using standard technology. The PDP can be broken down into two parts: top plate 10 and bottom plate 20. The top plate 10 has rows of paired electrodes referred to as the sustain electrodes 11a, 11b. The sustain electrodes are composed of wide transparent indium tin oxide (ITO) electrodes 12 and narrow Cr/Cu/Cr bus electrodes 13. These electrodes are formed using sputtering and multi-layer photolithography. The sustain electrodes 11 are covered with a thick (25 μm) dielectric layer 14 so that they are not exposed to the plasma. Silk-screening a high dielectric paste over the surface of the top plate and consolidating it in a high temperature process step forms this dielectric layer 14. A magnesium oxide layer (MgO) 15 is deposited by electron-beam evaporation over

the dielectric layer to enhance secondary emission of electrons and improve display efficiency. The bottom plate 20 has columns of address electrodes 21 formed by silk-screening silver paste and firing the paste in a high temperature process step. Barrier ribs 22 are then formed between the address electrodes 21. These ribs 22, typically 50 μm wide and 120 μm high, are formed using either a greater than ten layer multiple silk-screening process or a sandblasting process. In the sandblasting method, barrier rib paste is blade coated on the glass substrate. A photoresist film laminated on the paste is patterned by photolithography. The rib structure is formed by sandblasting the rib paste between the exposed pattern, followed by removal of the photoresist layer and a high temperature consolidation of the barrier rib 22. Alternating red 23R, green 23G, and blue 23B phosphors are silk-screened into the channels between the barrier ribs to provide color for the display. After silk-screening the phosphors 23, the bottom plate is sandblasted to remove excess phosphor in the channels. The top and bottom plates are frit sealed together and the panel is evacuated and backfilled with a gas mixture containing xenon.

The basic operation of the display requires a plasma discharge where the ionized xenon generates ultraviolet (UV) radiation. This UV light is absorbed by the phosphor and converted into visible light. To address a pixel in the display, an AC voltage is applied across the sustain electrodes 11 which is large enough to sustain a plasma, but not large enough to ignite one. A plasma is a lot like a transistor, as the voltage is increased nothing happens until a specific voltage is reached where it turns on. Then an additional short voltage pulse is applied to the address electrode 21, which adds to the sustain voltage and ignites the plasma by adding to the total local electric field, thereby breaking down the gas into a plasma. Once the plasma is formed, electrons are pulled out of the plasma and deposited on the MgO layer 15. These electrons are used to ignite the plasma in the next phase of the AC sustain electrodes. To turn the pixel off, an opposite voltage must be applied to the address electrode 21 to drain the electrons from the MgO layer 15, thereby leaving no priming charge to ignite the plasma in the next AC voltage cycle on the sustain electrodes. Using these priming electrons, each pixel can be systematically turned on or off. To achieve gray levels in a plasma display, each video frame is divided into 8 bits (256 levels) and, depending on the specific gray level, the pixels are turned on during these times.

There are presently three address modes of operation for a standard AC plasma display: (1) erase address (U.S. Pat. No. 5,446,344), (2) write address (U.S. Pat. No. 5,661,500), and (3) ramped voltage address (U.S. Pat. No. 5,745,086). The prior art wave forms for the matrix erase address waveform is shown in FIG. 2. In the initial address cycle CA in the line display period T a discharge sustain pulse PS is applied to the display electrode 11a and simultaneously a writing pulse in applied to the display electrode 11b. In FIG. 2, the inclined line in the discharge sustain pulse PS indicates that it is selectively applied to lines. By this operation, all surface discharge cells are made to be in a written state. After the discharge sustain pulses PS are alternately applied to the display electrodes 11a and 11b to stabilize the written states, and at an end stage of the address cycle CA, an erase pulse PD is applied to the display electrode 11b and a surface discharge occurs.

The erase pulse PD is short in pulse width, 1 μs to 2 μs . As a result, wall charges on a line as a unit are lost by the discharge caused by the erase pulse PD. However, by taking

FRIT-SEALING PROCESS USED IN MAKING DISPLAYS

REFERENCE TO RELATED APPLICATIONS

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5 MAKING DISPLAYS", which received a notice of allowance on June 5, 2001. The
aforementioned application is hereby incorporated herein by reference.

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